Substrate effects in sub-32 nm Ultra Thin SOI MOSFETs with Thin Buried Oxide

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1. Abstract

This paper underpins the influence of space-charge condition at the substrate / BOX interface, as a function of the gate length, on the front threshold voltage (V_{THf}) and subthreshold slope (S) of sub-32 nm Ultra Thin body (UTB) SOI MOSFETs with very thin buried oxide (UTB²).

2. Introduction

UTB FD-SOI MOSFETs are very attractive to reduce short channel effects (SCE) **[1]**, but may be degraded by self-heating and coupling between channel potential and drain bias, by fringing fields through the silicon film, BOX and Si substrate **[2-4]**. Thin BOX has then been proposed to solve these problems.

Our work demonstrates that while UTB^2 can indeed achieve better performance for several parameters, a particular attention has to be paid to the substrate space-charge condition and couplings of body with source, drain and bulk which dramatically modify the electrical parameters as a function of gate length.

3. Devices description

Structures used for this study are FD-SOI transistors processed at CEA-LETI on both standard 145 nm-thick SiO_2 buried oxide and extremely thin BOX of 11.5 nm. (100) SOI wafers have been thinned down to T_{Si} = 11 nm and integrated with the FD-SOI CMOS process described in [4] (with TiN/HfO2, EOT = 17.5 Å). Gate lengths from 1 µm down to 25 nm are available.

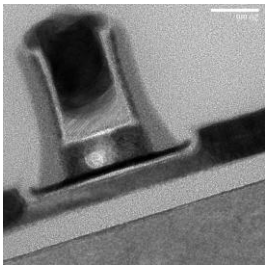

Fig. 1: *TEM picture of the studied 25 nm UTB² structure.*

4. Experimental and simulation results

Fig. 2(a&b) presents the front threshold voltage (V_{THf}) extracted by the double derivative method on drain current (I_D) – front gate voltage (V_G) characteristics at low drain voltage (V_D) as a function of substrate voltage (V_{SUB}) and gate length (L_G). All V_{THf} curves demonstrate the linear dependence on V_{SUB}, typical of FD SOI MOSFETs. However a clear plateau appears for V_{SUB} between 0 V and 1 V (***Fig.2(a)***) which following **[5]** can be related to depletion conditions at the BOX / substrate interface. In such case, the V_{SUB} sweep is compensated by the variation of the potential drop in the depletion region flattening the V_{THf} curve.

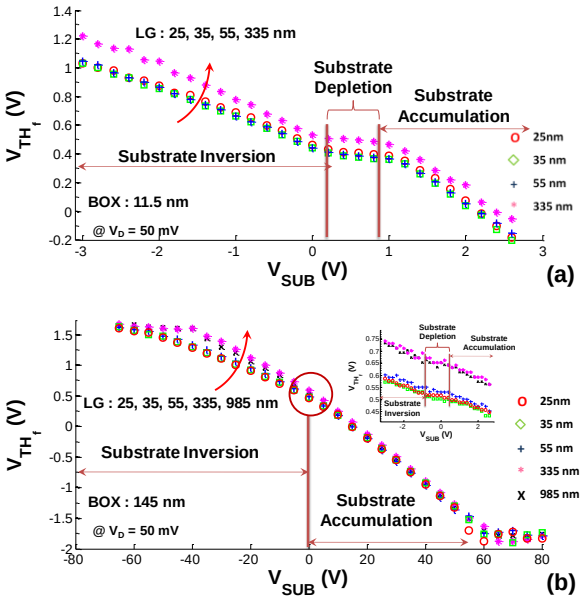

Fig. 2: *Threshold voltage extracted for different gate lengths as a function of the substrate bias voltage and for the two studied BOX thicknesses. V_{SUB} is varying from −3 V to +3 V for the 11.5 nm thick BOX and from -80 V to +80V for the 145 nm one.*

The effect can also be seen in the 145 nm thick BOX MOSFETs but is less noticeable due to the much larger V_{SUB} range typically used to shift the film / BOX interface from accumulation to inversion corresponding to the well-known respective top and bottom plateaus of the V_{THf}-V_{SUB} curve. In the devices with ultra thin film and BOX (UTB²), these last plateaus could not be observed, meaning that back film accumulation or inversion cannot be sustained out of the control of the front gate voltage **[6]**.

In ***Fig.2***, we also notice that the V_{THf}-V_{SUB} slope is larger in substrate accumulation resulting in higher body effect than in substrate inversion. In the latter case, the

effect is even less pronounced for short channel devices, suggesting partial screening of the substrate coupling. Further confirmation of these effects is derived from the subthreshold slope (S) analysis which is presented in ***Fig. 3*** as a function of V_{SUB} and L_G for the UTB² devices and can be explained as follows. The influence of V_{SUB} is twofold: in addition to changing the space charge conditions in the substrate, it also changes the channel position in the film. Negative V_{SUB} pushes the channel to the front film interface which minimizes S, while it is degraded by positive V_{SUB} attracting the channel at the back interface.

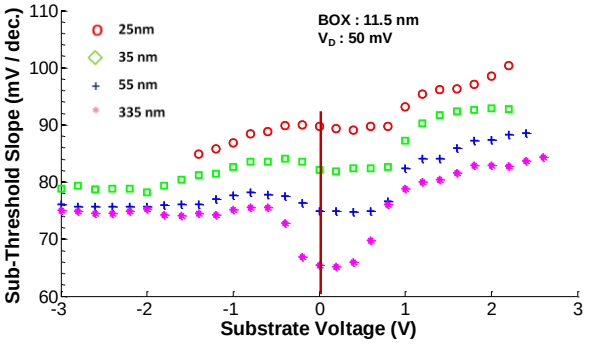

Fig. 3: *Subthreshold slope (S) of UTB² transistors extracted from ID-VG @ V_D = 20 mV for five selected gate lengths.*

This has been confirmed by 2-D numerical simulations (***Fig. 4.a***, ***inset***). Furthermore, the degradation of S observed for increasing V_{SUB} from -2 to +3 V for the long-channel MOSFET is in excellent quantitative agreement with Colinge's model **[7]** taking the variation of the channel depth into account. In the substrate depletion regime, the channel position varies less with V_{SUB} (***inset*** of ***Fig. 4.a***) as the potential at the BOX / substrate remains almost constant as shown by V_{THf}. However, the simulations show a L_G-dependence since weak inversion at the BOX/substrate interface under the N^+-doped source/drain regions propagates laterally and raises the BOX/SUB potential for short length (***Fig. 4b***).

In addition, the dip of S clearly observed around V_{SUB} = 0 V for the 335 nm device is also in fair agreement with depletion extension in the substrate as it reduces the vertical coupling between channel and ground. This dip lessens and even vanishes for short-channel transistors when the lateral coupling to source and drain through BOX and substrate supersedes the vertical coupling to the back contact, as already mentioned from the V_{THf} observations. 2D simulations (***Fig. 4b***) confirm that the substrate depletion is reduced for shorter transistors. Finally, the global increase of S with L_G reduction is also in good quantitative agreement with Skotnicki's model **[8]** taking the effective oxide thickness into account. As the latter is larger for positive V_{SUB}, it indeed leads to higher short-channel S degradation.

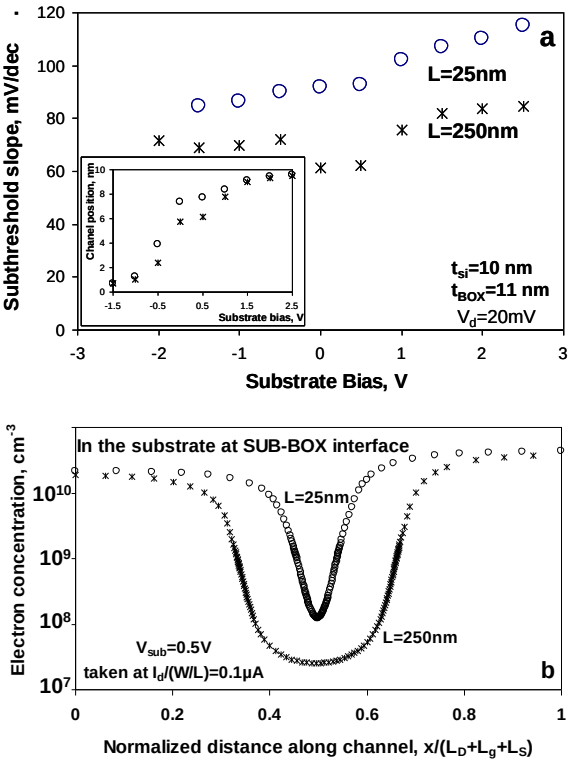

Fig. 4: *2D Atlas simulations:* ***(a)*** *S vs. V_{SUB} for UTB² MOSFET with lengths of 25 and 250nm. V_D=20mV. Insert gives depth of channel ("zero" corresponds to gate dielectric / Si interface, 10 nm to Si film / BOX interface).* ***(b)*** *electrons concentration at the BOX-SUB interface as a function of normalized distance along channel length (L_S=L_D=0.3µm), V_{SUB}=0.5V, taken at I_D/(W/L)=0.1µA.*

6. Conclusions

This work reveals the peculiarities of the conditions at the BOX / substrate interface and their length dependence, on the operation of ultra thin film and buried oxide FD SOI MOSFETs, suggesting the need for the adaptation of compact models.

Acknowledgements

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